JTAG

1st Revision: 2007/8/17
2nd Revision: 2013/3/17
3rd Revision: 2019/11/21

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What's JTAG

- Joint Test Action Group
- Also known as "Boundary-Scan"
- Standards Cluster:
  - IEEE Std 1149.1 (1990, 2001) **IEEE Standard Test Access Port and Boundary-Scan Architecture**
  - IEEE Std 1149.4 (1999) **IEEE Standard for a Mixed-Signal Test Bus**
  - IEEE Std 1149.5 (1995) **IEEE Standard for Module Test and Maintenance Bus**
  - IEEE Std 1149.6 (2003) **IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks**
  - IEEE Std 1149.7 (2009) **IEEE Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary-Scan Architecture**

Why JTAG

- Test
  - The Incredible Shrinking Board
  - The Ever-Expanding Chip
  - Can't Afford Not To Test
- Standardization
- and more…

Functions of JTAG

- Test
  - External Test: Interconnect Test, Logic Cluster Test
  - Internal Test
- Programming/Configuration
  - Lattice: ispVM, ispVME , …
  - Xilinx: iMPACT, …
  - Altera: Max+plus II Programmer, …
  - IEEE Std 1532 **IEEE Standard for In-System Configuration of Programmable Devices**
- Debug
  - ICE(In Circuit Emulation): CPU, DSP, ...
  - FPGA: Xilinx ChipScope & LA, Altera SignalTap, ...

How to JTAG - 1

- Hardware Interface
  - Pin
    - TDI
    - TCK
    - TMS
    - TDO
    - TRST (Optional)
  - Mechanical
    - Altera
    - Xilinx
    - Lattice
    - ARM
    - MIPS EJTAG
    - Freescale COP
    - …

How to JTAG - 2

- TAP Controller State Machine

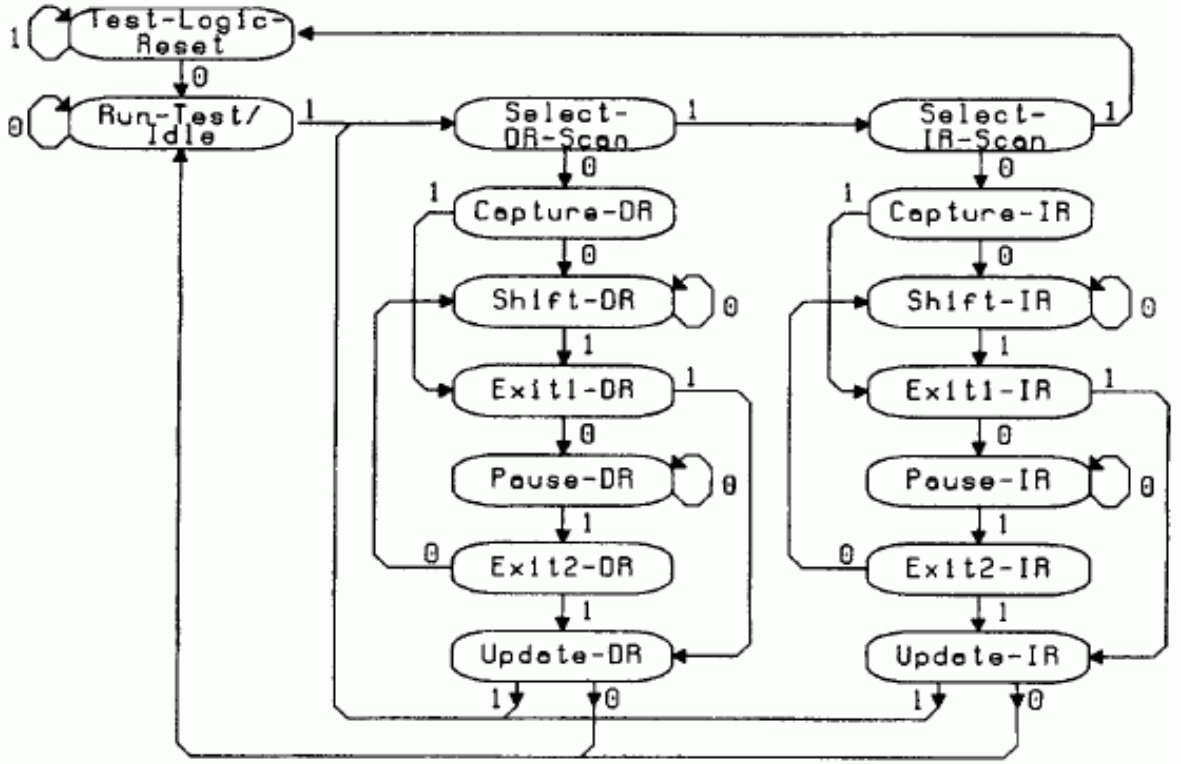


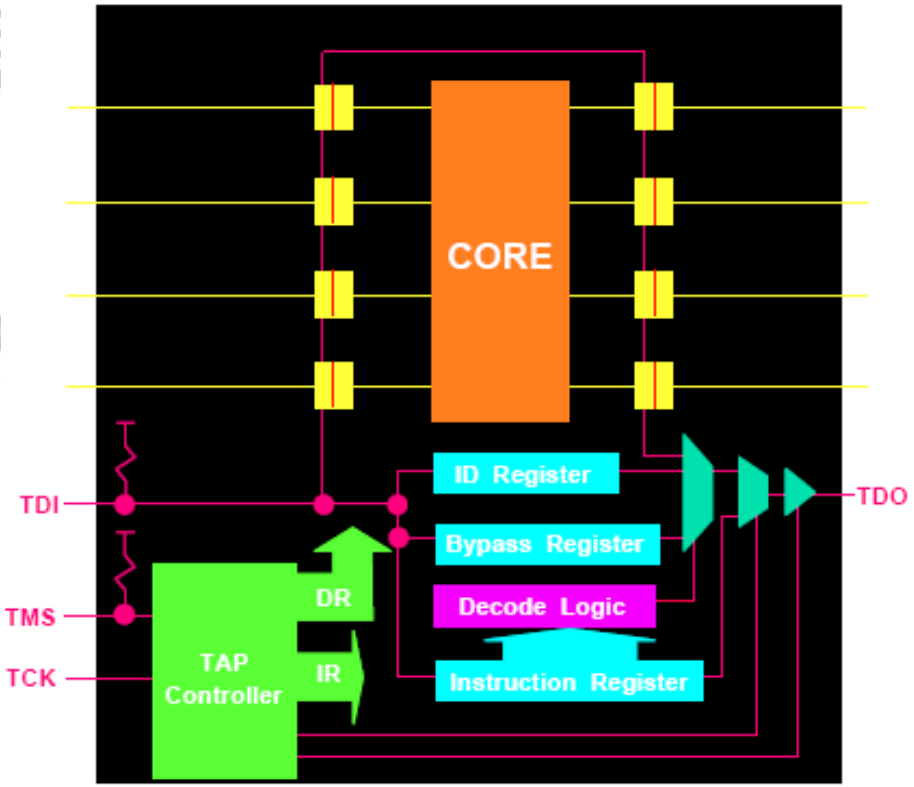
Figure 6-1—TAP controller state diagram

How to JTAG - 3

- BSDL (Boundary Scan Description Language)
  - Overview
    - A subset and standard practice of the VHSIC Hardware Description Language (VHDL) (IEEE Std 1076-1993)
  - Key Info
    - Instructions
      - Mandatory: SAMPLE, PRELOAD, EXTEST, BYPASS
      - Optional: HIGHZ, IDCODE, CLAMP
    - BSC
      - Format: num cell port function safe [ccell disval rslt]
    - Boundary length, IDCODE register, and so on
  - Example

Inside JTAG

- The Control Architecture
  - Boundary scan and other test data registers operate under control of instruction register
  - Data is scanned from TDI to TDO through selected test data register or instruction register under control of Test Access Port (TAP) controller
  - TAP operates synchronously to TCK using TMS for state selection



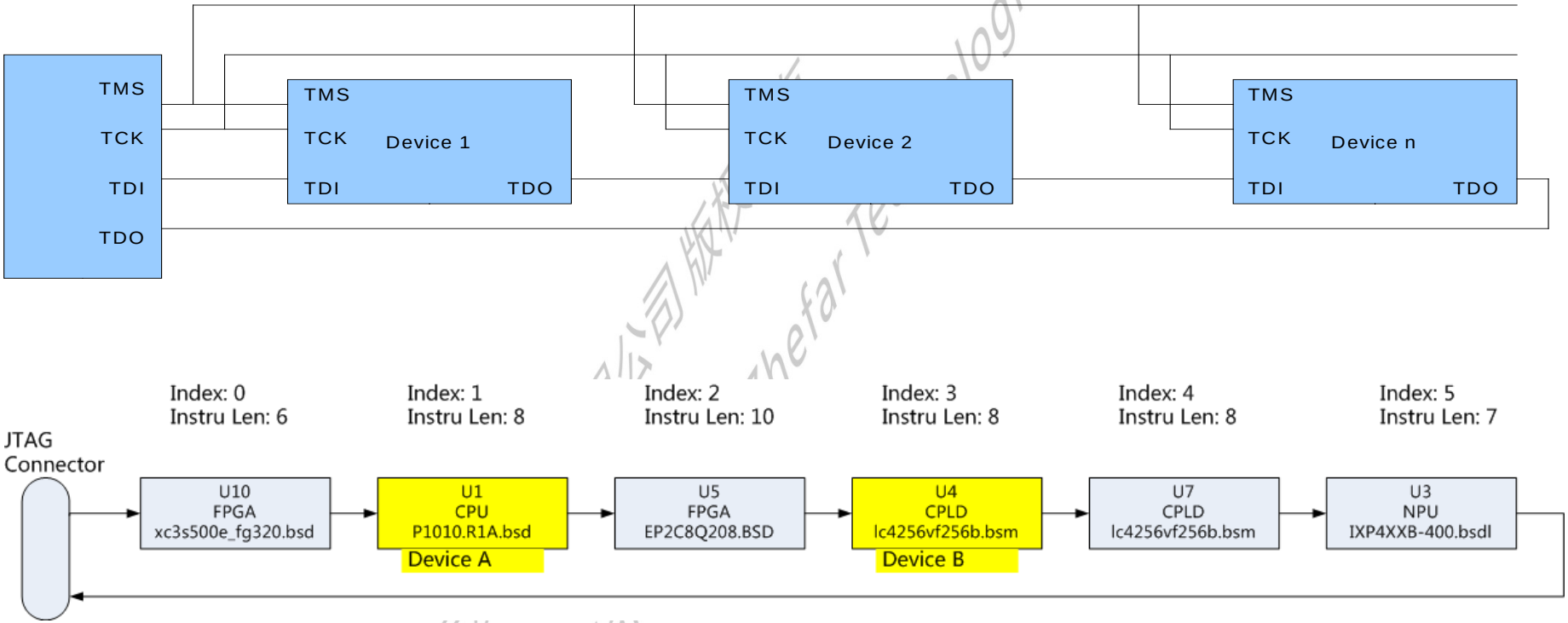
JTAG Instructions

Instruction	Status
BYPASS	Mandatory
CLAMP	Optional
EXTEST	Mandatory
HIGHZ	Optional
IDCODE	Optional
INTEST	Optional
RUNBIST	Optional
SAMPLE / PRELOAD	Mandatory
USERCODE	Optional

How do we use JTAG

- Device vendor
  - See previous "*Functions of JTAG*"
- Criterion
  - Electric & Mechanical
  - Explain:
    - See document
- Applications
  - JTAG Flash Programmer
  - Boundary Scan Test

JTAG Chain



How to scan a JTAG chain

- Question: How many devices?
  - Answer: Use BYPASS instruction
    - New question: I don't know what device it is, how to send its BYPASS instruction?
      - Answer:
- Question: What are they?
  - Answer: Use IDCODE instruction
    - New question: What's the value of IDCODE instruction? We are not so lucky this time because IDCODE instruction is not standard.
      - Answer: There should be a way.
  - IDCODE Register Format

Version	Device ID	MFG	Mandatory
4 bits	16 bits	11 bits	1

How to Program via JTAG

- JTAG Device itself, like CPLD/FPGA and MCU
  - User defined
  - IEEE Std 1532
- Device connected to JTAG device, like Flash
  - EXTEST

Discuss on JTAG Flash Programmer

- How it works?
- Benefits

References

- IEEE. IEEE Standard Test Access Port and Boundary-Scan Architecture. IEEE Std 1149.1-2001, 14 June 2001.
- TI Test Symposium. JTAG (IEEE 1149.1/P1149.4) Tutorial - Introductory, 1997.
- DALLAS-MAXIM. DS26303 datasheet. Aug 23, 2006.

The End

- Q & A

Thank you!

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